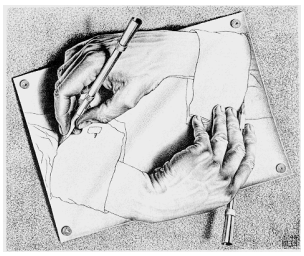
ECE 5530: Configurable Computing – Spring 2010



Instructor: Dr. Cameron Patterson
Office: 2040J Torgersen Hall
Email: cdp@vt.edu

Lectures: Tuesday/Thursday 9:30AM – 10:45AM
in Whittemore 281

Course material: posted on Scholar

Office Hours: by appointment (send e-mail).

E-mail: Prefix the subject line with [5530].
Only formal and complete messages will be answered.

Course Objectives

The von Neumann architecture has had a good run and continues to serve us well for many computing needs. However, application specific architectures are sometimes needed to reach the performance desired on platforms ranging from embedded systems to supercomputers. Traditionally, ASICs have been used in these situations, but the development time (> 1 year), cost (> $50M), risk and inflexibility often rule them out. The ideal is an inexpensive, high performance, low power, and easy to program system permitting the computation, communication and control structures to be quickly customized an unlimited number of times. Marketing aside, no platform currently fulfills all of these objectives. We will study a variety of architectures that address several of the goals, and examine the tradeoffs made. Performance and ease of use are especially hard to satisfy simultaneously, partly because hardware synthesis and optimization are inherently more difficult than generating sequential code for a fixed instruction set.

Prerequisites

The official prerequisites are ECE 4514 (Digital Design II) or equivalent, and ECE 5504 (Computer Architecture) or equivalent. Students are required to:

- have the ability to model, test and evaluate FPGA-based hardware systems,
- have a thorough understanding of computer organization and networks, along with the ability to design and evaluate performance metrics for such systems.

The three warm-up assignments will consist of implementing a parallel algorithm on a GPU, FPGA, and multi-core CPU architectures. The project will require proficiency developing hardware and software components, tools and applications.

References and Tools

Presentations, notes and papers will be posted on Scholar.

Accounts will be provided on a high performance, 64-bit Ubuntu workstation: a Dell Studio XPS 435 (since relabeled as the XPS 9000) with a Core i7 processor, 8GB of DDR3 memory, and 1TB of RAID1 disk storage. Direct `ssh` access through a hardware firewall will be provided. The workstation has all necessary tools installed, although you are encouraged to install the tools on your own PC. The Studio XPS has the following PCIe and PCI cards:

- 220 watt Nvidia GeForce GTX 275 CUDA-enabled GPU with 900MB GDDR3 memory, 240 cores, and over 1TFLOP of floating point performance.
- $10k Alpha Data ADM-XRC-4FX board containing an XC4VFX100 FPGA. A software API provides efficient DMA data transfers between the host CPU and FPGA.

Cell Phones and Pagers must be turned off during lecture, no exceptions.

Honor Code Requirements

The instructor of this course supports the Virginia Tech Graduate Honor System. Unless designated as a team project, all work should be done individually. Copying of another person's work or submitting anyone else's work as your own will be treated as honor code violations. It is also a violation to give unauthorized assistance. All potential honor code violations will be reported to the Graduate Honor System. Your course instructor will be happy to discuss Honor System questions with you.

Grade Determination

10%	Class participation
45%	Three assignments: implement a parallel algorithm on CPU, GPU and FPGA architectures.
10–15%	Bonus: partition the algorithm over more than one architecture.
	Project
10%	Proposal
10%	Milestones
10%	Demonstration
15%	Paper

For the project deliverables, full points correspond to conference quality work, results and presentation. Most student projects will contribute components (such as module generators) to the openHCA (Hardware Communication Architecture) IDE for FPGA-based implementation of streaming applications. A paper describing openHCA will be provided in class.

Course and Project Themes

- FPGA architectures and run-time reconfiguration
- Multicore systems
- Datapath architectures including GPGPUs and CGRAs
- Streaming computation and communication
- Hybrid computing
- Configurable communication
- Software defined radio platforms
- Virtual hardware
- Tools and run-time CAD algorithms
- Applications

Accommodation

Reasonable accommodations are available for students who have documentation of a disability from a qualified professional. Students should work through Services for Students with Disabilities (SSD) in Kent Square. Any student with accommodations through the SSD Office should contact me during the first two weeks of the semester.

If participation in some part of this class conflicts with your observation of specific religious holidays during the semester, please contact me during the first two weeks of class to make alternative arrangements.

If you miss class due to illness, especially in the case of some deadline, see a professional in Schiffert Health Center. If deemed appropriate, documentation of your illness will be sent to the Dean's Office for distribution to me.

If you experience a personal or family emergency that necessitates missing class, contact the Dean of Students at 231-3787 or visit 109 E. Eggleston Hall.